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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,265	03/09/2001	Yoshitaka Tsunashima	790001-2002	7077

20999 7590 05/21/2003

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	8

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/803,265	Applicant(s) TSUNASHIMA ET AL.	
	Examiner Jennifer M. Dolan	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,12,13 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5 and 24* is/are allowed.

6)☒ Claim(s) *1-4, 12, 13,21-23, and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action is in response to Amdt. A, filed 2/24/03.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 23 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 6,020,243 to Wallace et al.

Wallace discloses a semiconductor device comprising a semiconductor substrate (20) and a gate insulating film (ZrSiON or HfSiON films) provided on the semiconductor substrate (column 2, lines 45-61 and column 6, lines 32-55). At least part of the insulating film is considered to contain a metal oxide film, because the film is compositionally graded such that it is nearly a pure metal oxynitride at the top of the insulating film layer (column 6, lines 50-54; column 9, lines 7-27). Wallace further discloses a single insulating film (ZrSiON or HfSiON films) containing metal, silicon, and oxygen provided between the semiconductor substrate and the metal oxide film portion of the ZrSiON (column 6, lines 32-54; column 9, lines 7-27), where nitrogen is contained in the single insulating film containing metal, silicon, and oxygen (column 6, lines 32-54).

Assuming arguendo, the top, ZrO-rich portion of the film cannot be considered to be "at least part of the gate insulating film including a metal oxide film."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the gate insulating film of Wallace comprises a separate metal oxide film and single insulating film, such that the single insulating film is between the substrate and the metal oxide film. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide separate metal oxide and single insulating films, because they would have substantially the same compositional profile as the graded layer of Wallace. Since Wallace already shows that it is advantageous to have a gate insulating film which is primarily Zr-oxynitride at the top of the film, and containing Si, Zr, O, and N between the Zr-oxynitride and the substrate, it is well within the purview of a person skilled in the art to recognize that the Zr-oxynitride portion of the insulating film could be placed in a separate 'layer' without really changing the device structure, profile, composition, or performance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 –3, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al. in view of U.S. Patent No. 6,274,905 to Mo.

Regarding claim 1, Wallace discloses a semiconductor device (figure 1; column 1, lines 15-44) comprising: a semiconductor substrate (20); and a gate insulating film (column 2, lines

28-30) provided on the substrate, at least part of which includes an insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58); wherein nitrogen is contained in the insulating film containing metal, silicon, and oxygen (column 2, lines 28-58).

Wallace fails to disclose that fluorine is contained in the insulating film.

Mo discloses advantages for placing fluorine in a gate insulating film (column 4, lines 54-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate insulating film of Wallace, such that it includes fluorine, as taught by Mo. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide fluorine in the gate dielectric, because the fluorine passivates the surface of the gate dielectric, resulting in a gate dielectric that is more stable and robust, and less likely to experience current leakage due to stress (Mo, column 4, lines 54-64).

Regarding claim 2, Wallace discloses a semiconductor device comprising a semiconductor substrate (20) and a gate insulating film (ZrSiON or HfSiON films) provided on the semiconductor substrate (column 2, lines 45-61 and column 6, lines 32-55). At least part of the insulating film is considered to contain a metal oxide film, because the film is compositionally graded such that it is nearly a pure metal oxynitride at the top of the insulating film layer (column 6, lines 50-54; column 9, lines 7-27). Wallace further discloses a single insulating film (ZrSiON or HfSiON films) containing metal, silicon, and oxygen provided between the semiconductor substrate and the metal oxide film portion of the ZrSiON (column 6, lines 32-54; column 9, lines 7-27), where nitrogen is contained in the single insulating film containing metal, silicon, and oxygen (column 6, lines 32-54).

Wallace fails to disclose fluorine in the insulating film. Additionally, assuming arguendo, the top, ZrO-rich portion of the film cannot be considered to be "at least part of the gate insulating film including a metal oxide film."

Mo discloses advantages for placing fluorine in a gate insulating film (column 4, lines 54-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the gate insulating film of Wallace contains fluorine, as taught by Mo, and comprises a separate metal oxide film and single insulating film, such that the single insulating film is between the substrate and the metal oxide film. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide fluorine in the gate dielectric, because the fluorine passivates the surface of the gate dielectric, resulting in a gate dielectric that is more stable and robust, and less likely to experience current leakage due to stress (Mo, column 4, lines 54-64). Additionally, one skilled in the art would have been motivated to provide separate metal oxide and single insulating films, because they would have substantially the same compositional profile as the graded layer of Wallace. Since Wallace already shows that it is advantageous to have a gate insulating film which is primarily Zr-oxynitride at the top of the film, and containing Si, Zr, O, and N between the Zr-oxynitride and the substrate, it is well within the purview of a person skilled in the art to recognize that the Zr-oxynitride portion of the insulating film could be placed in a separate 'layer' without really changing the device structure, profile, composition, or performance.

Regarding claim 3, Wallace discloses that the insulating film is amorphous (column 6, lines 32-34).

Regarding claims 21 and 22, Wallace discloses that the substrate is silicon (column 4, lines 12-18).

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al. in view of Mo as applied to claim 3 above, and further in view of U.S. Patent No. 6,407,435 to Ma et al.

Wallace fails to disclose a flat insulating film having an opening portion in which the films are formed.

Ma discloses a flat insulating film (311; figures 6-8) having a gate opening portion (300) in which the amorphous metal oxide film (topmost instance of 340) and the gate insulating film containing metal, silicon, and oxygen (bottommost instance of 330 and 340) are formed; and a gate electrode (418) formed on the gate insulating film in the gate opening portion and having a surface which is flush with the flat insulating film (figure 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Wallace, such that it is formed in the 'substitute gate structure' taught by Ma. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to use the structure taught by Ma, because Ma shows that it is an equivalent gate structure (see figures 1-8), and has the additional benefit of being usable in 'substitute gate' manufacturing methods, as well as having a reduced device height (column 5, lines 16-29; figures 4-8).

6. Claims 12, 13, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al. in view of U.S. Patent No. 6,261,887 to Rodder and further in view of Mo.

Regarding claim 12, Wallace discloses a semiconductor device comprising: a semiconductor substrate (column 4, lines 14-15); transistor regions having a gate insulating film (36) at least a part of which includes an insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58), where the composition ratios of the metal elements, silicon, and oxygen are the same across the substrate.

Wallace fails to disclose distinct first and second transistor regions wherein the composition ratios in the gate insulating films in the first and second regions are different. Wallace further fails to disclose that at least one of the insulating films contains fluorine.

Rodder discloses distinct first and second transistor regions (16 and 18; column 4, lines 19-30), wherein the gate insulating films have different compositions/dielectric constants (column 11, lines 30-60).

Mo discloses advantages for placing fluorine in a gate insulating film (column 4, lines 54-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wallace, such that first and second transistor regions are provided, where the composition ratios of the gate dielectric are different in the first and second regions, as taught by Rodder, and that fluorine is present in the gate insulating layer, as taught by Mo. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide first and second transistor regions, because for CMOS technology, which is useful for low-dissipation logic circuits, both npn and

pnp transistor regions need to be provided and separately optimized (Rodder, column 1, lines 32-44). One further would have been motivated to provide gate insulation layers which differ in concentration between the two regions, because the two regions need gate layers with different work functions and threshold voltages, and a person skilled in the art would recognize that changing the composition ratios of the material in the two regions would change the dielectric constant, and thus allow for separate optimization of the work function and threshold voltage in each region, without introducing new materials into the fabrication procedure (Rodder, column 11, lines 30-60). A person having ordinary skill would further have been motivated to provide fluorine in the insulating film, because the fluorine passivates the surface of the gate dielectric, resulting in a gate dielectric that is more stable and robust, and less likely to experience current leakage due to stress (Mo, column 4, lines 54-64).

Regarding claim 13, Wallace discloses a semiconductor device comprising: a semiconductor substrate (column 4, lines 14-15); and transistor regions having a gate insulating film (36) at least a part of which includes an insulating film containing metal, silicon, and oxygen (column 2, lines 28-30; lines 45-58), provided across the whole substrate. The insulating film containing metal, silicon, and oxygen is a metal oxide film.

Wallace fails to disclose distinct first and second transistor regions.

Rodder discloses distinct first and second transistor regions (16 and 18; column 4, lines 19-30).

Mo discloses advantages for placing fluorine in a gate insulating film (column 4, lines 54-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Wallace, such that first and second transistor regions are provided, as taught by Rodder, and such that fluorine is provided in the gate insulator, as taught by Mo. The rationale is as follows: One of ordinary skill in the art at the time the invention was made would have been motivated to provide first and second transistor regions, because for CMOS technology, which is useful for low-dissipation logic circuits, both npn and pnp transistor regions need to be provided and separately optimized (Rodder, column 1, lines 32-44). Additionally, a person skilled in the art would have been motivated to provide fluorine in the gate insulating layer, because the fluorine passivates the surface of the gate dielectric, resulting in a gate dielectric that is more stable and robust, and less likely to experience current leakage due to stress (Mo, column 4, lines 54-64).

Regarding claim 25, Wallace discloses that the substrate is silicon (column 4, lines 12-18).

Allowable Subject Matter

7. Claims 5 and 24 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record, considered as a whole, fails to teach or suggest making a fluorine-containing silicate and a metal oxide for gate insulation using different metal elements for the silicate and the metal oxide.

The closest art of record is U.S. Patent No. 6,057,584 to Gardner et al., which suggests a gate insulating layer using two layers of metal oxide, wherein different metals are used for each

layer, but doesn't suggest that one of the layers is a fluorine-containing silicate. U.S. Patent No. 6,020,243 to Wallace et al. suggests a gate insulating layer comprising a fluorine-containing silicate and a metal oxide, but there is no motivation to combine the references, such that a metal silicate and a metal oxide use different metals.

Changing the composition of the two layers improves upon the prior art by allowing for a wide selection of gate insulator thicknesses, dielectric constants, and bonding properties with the silicon substrate and gate electrode layers.

Response to Arguments

9. Applicant's arguments with respect to all of the claims have been considered but are moot in view of the new grounds of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (703) 305-3233. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd
May 13, 2003

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800